REMARKS

Claims 13 and 21 have been amended and claims 13-23 remain pending in the present application. Applicants submit that no new matter is being added to the present application by these amendments.

Independent claims 13 and 21 have been amended to distinguish over the Choi et al., "High Speed Pattern Matching For A Fast Huffman Decoder" (February 1995) reference cited by Applicants.

By way of background, the variable length table decoder (186) of th present invention, as recited in independent claim 13, provides for decoding of compressed video data using variable length code tables. The compressed video data includes variable length encoded data which represents an image area of a transmitted frame. The variable length table decoder (186) is coupled to a memory (156A, 156B) which stores variable length encoded data and also to a shifter circuit (164) associated with the memory (156A, 156B) which makes a predetermined number of bits (162) of the variable length encoded data visible.

The variable length table decoder (186) includes a pattern match circuit (188) coupled to the memory (156A, 156B) and to the shifter circuit (164) for identifying a unique prefix pattern in the variable length encoded data (162) made visible by the shifter circuit (164). Each unique prefix pattern has a prefix pattern length which may be the same as or different from the prefix pattern length of other unique prefix patterns as shown in Fig. 4. Variable length code table data

is provided which includes a decoded value associated with each of a plurality of variable length codes. In particular, the variable length code table data comprises a plurality of subtable data circuits which are each associated with a unique prefix pattern in the variable length codes and independent of the prefix pattern length. A datapath (196) is provided to couple the variable length encoded data (162) made visible by the shifter circuit (164) to the pattern match circuit (188) and to each of the subtable data circuits for simultaneously applying the variable length encoded data (162) to the pattern match circuit (188) and to each of the subtable data circuits. Control circuitry (190, 192) is responsive to the pattern match circuit (188) for obtaining a decoded value (198) from the subtable data circuit associated with the unique prefix pattern in the variable length codes that matches the identified prefix pattern in the variable length encoded data, and additional data in the variable length codes after the unique prefix pattern that matches additional data in the variable length encoded data after the identified prefix pattern. This aspect of the invention is described in the specification at page 22, line 18 through page 24, line 9.

Choi et al. is directed to a variable length table decoder which includes a first Pattern Matching Unit 1 for identifying a unique prefix pattern in a slice of variable length encoded data and a second Pattern Matching Unit 2 for providing a decoded word from a plurality of subtable data circuits as shown in Fig. 7 of Choi t al.

In the variable length decoder of Choi et al., each unique prefix pattern (referred to as "first cluster") has a unique prefix pattern length (referred to as "first cluster codeword length") as shown in Table 1 of Choi et al. The subtable data circuits of the Pattern Matching Unit 2 are partitioned by the codeword length of the first cluster (see page 102, second paragraph, of Choi et al.) and use the other data in the variable length encoded data (referred to as "second cluster") to generate a decoded word. In this way, the variable length table decoder of Choi et al. identifies the codeword length of the prefix pattern (the "first cluster") and uses the subtable data circuit associated with the identified codeword length and the "second cluster" data to generate the decoded word.

Independent claim 13 has been amended to distinguish over the Choi et al. reference by reciting that the plurality of subtable data circuits of the variable length table decoder are each associated with a unique prefix pattern in the variable length codes "and independent of the prefix pattern length".

As shown in Fig. 4 of the present application, and in contrast to the variable length table decoder of Choi et al., the subtable data circuits of the present invention are partitioned by the unique prefix patterns in the variable length encoded data, and independent of prefix pattern length, such that two subtable data circuits, each associated with a unique prefix pattern, may have the same prefix pattern length (e.g., subtables K_{4_1} and K_{4_0} or subtables K_{5_001} and K_{5_000}).

In this way, the variable length table decoder of the present invention selects the proper subtable data circuit upon identifying the unique prefix pattern and thereby eliminates the additional step of identifying the codeword length of the prefix pattern (the "first cluster") as required in the variable length table decoder of Choi et al. This claimed feature, as recited in amended independent claim 13, is not taught or suggested by the Choi et al. reference. Similar amendments have been made to independent claim 21 to distinguish that claim over the cited Choi et al. reference as well.

Applicants believe that no fees are due. However, if any fees are deemed necessary to complete this communication, the Commissioner is hereby authorized to charge same to Deposit Account No. 23-3000.

Respectfully submitted,

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